The listing of claims will replace all prior versions, and listings, of claims in the application:

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Listing of Claims:

1. **(Currently Amended)** A magnetic random access memory (MRAM) device, comprising:

an array of magnetic memory cells that store data as different values of impedance;

a grid of bit and word lines for selectively accessing data in the array of magnetic memory cells; and

a plurality of corresponding resistors each placed in series with ones of the magnetic memory cells and the bit and word lines each of the plurality of corresponding resistors **having a cross-section smaller than that of the magnetic memory cells**;

wherein, the corresponding resistors cause localized heating of selected ones of the magnetic memory cells that assists in their switching.

2. (Original) The MRAM of claim 1 wherein:

the plurality of corresponding resistors are such that the thermal conduction path is modified to reduce heatsinking of the selected ones of the magnetic memory cells into the grid of bit and word lines.

3. (Original) The MRAM of claim 1 wherein:

the plurality of corresponding resistors are such that the electrical conductivity is modified to cause electro-resistive heating of the selected ones of the magnetic memory cells.

4. (Original) The MRAM of claim 1 wherein:

the plurality of corresponding resistors are such that the electrical conductivity is modified to cause electro-resistive heating of the selected ones of the magnetic memory cells, each spacer having a connection face that has a perimeter portion that is electrically conductive and a core portion that is thermally insulating so as to form barriers for heat conduction from the memory cells thereby easing cell state switching.

5. (Original) The MRAM as claimed in claim 4 wherein the conductive perimeter portion has a cross-sectional area smaller than that of the memory cell.

6. (Original) The MRAM of claim 3 wherein:

the electrically conducting perimeter portion is created by an isotropic etch process that removes electrically conductive material from a core portion of the spacer.

7. (Original) The MRAM of claim 6 wherein:

the electrically conducting perimeter portion comprises a narrow ridge of conductive material through which electrical connection to the memory cell is established.

8. (Original) The MRAM of claim 1, wherein:

the plurality of corresponding resistors comprise a plurality of spacers, each spacer connecting a line with a respective one of said magnetic memory cells, each spacer having a connection face that has a perimeter portion that is electrically conductive so as to form barriers for heat conduction from the memory cells thereby easing cell state switching.

9. (Original) The MRAM in claim 8 wherein the conductive core portion has a cross-sectional area smaller than that of the memory cell.

10. (Original) The MRAM in claim 8 wherein:

The electrically conductive core portion is formed by etching a hole into an insulating material using an isotropic etch process and filling the hole with an electrically conductive material through which connection to the memory cells is established.

11~~12~~. **(Currently Amended)** The MRAM of claim 1, wherein:

the plurality of corresponding resistors comprise a plurality of spacers, each spacer connecting a line with a respective one of said magnetic memory cells, each spacer having a connection face that uses a thermally insulating material so as to

form barriers for heat conduction from the memory cells thereby easing cell state switching.

12~~13~~. **(Currently Amended)** The MRAM of claim 1, wherein:

the corresponding resistors are formed as areas of reduced cross-section of the lines in the grid.

13~~14~~. **(Currently Amended)** The MRAM of claim 12 ~~13~~ wherein:

the reduced cross-sectional area is created by reducing the thickness of one or more conductor lines in the region adjacent one or more magnetic memory cells.

14~~15~~. **(Currently Amended)** The MRAM of claim 12 ~~13~~ wherein:

the reduced cross-sectional area is created by narrowing the width of one or more conductor lines in the region adjacent one or more magnetic memory cells.

15~~16~~. **(Currently Amended)** A magnetic random access memory (MRAM) device, comprising:

an array of magnetic memory cells that store data as different values of impedance;

a grid of bit and word lines for selectively accessing data in the array of magnetic memory cells; and

a plurality of spacers, each spacer connecting a line with a respective one of said magnetic memory cells, each spacer having a connection face that has a recess which is filled with an electrically insulating material to increase the electrical resistance of the spacers to generate heat when a current passes through the spacers which can be utilized to ease cell state switching.

16~~17~~. **(Currently Amended)** A magnetic random access memory (MRAM) device, comprising:

an array of magnetic memory cells that store data as different values of impedance;

a grid of bit and word lines for selectively accessing data in the array of magnetic memory cell, the grid having a plurality of thermally and electrically resistive portions which provide connections to the

magnetic memory cells **each of the plurality of thermally and electrically resistive portions having a cross-section smaller than that of the magnetic memory cells**; and

wherein the resistive portions increase the thermal resistance for heat generated by each memory cell and during operation provide localized heating of active memory cells to ease cell state switching.

17~~18~~. Previously withdrawn from consideration.

18~~19~~. **(Currently Amended)** A method for operating MRAM devices, comprising:

conducting an electrical current through narrow portions of a spacer that connects memory cells of an MRAM array with bit and word lines so that heat is resistively generated in the narrow portions **wherein the spacer has a cross-section smaller than that of the memory cells**; and

using the generated heat to ease cell state switching of memory cells.

19~~20~~. Previously withdrawn from consideration.